EXHIBIT H

PWR-SMP3

PWM Power Supply IC

120 VAC Input
Isolated, Regulated DC Output

POWER INTEGRATIONS, INC.

Product Highlights

Integrated Power Switch and CMOS Controller
- Output power up to 3 W from 120 VAC input
- Integrated solution minimizes overall size
- External transformer provides isolation and selectable output voltages

High-voltage, Low-capacitance MOSFET Output
- Designed for 120 VAC off-line applications
- Can also be used with DC inputs from 36 V to 200 V
- Low capacitance allows for high frequency operation

High-speed Voltage-mode PWM Controller
- Internal pre-regulator self-powers the IC during start-up
- High PWM frequency reduces component size
- Minimum external parts required

Built-In Self-protection Circuits
- Inherent current limiting protects from short-circuits
- Input overvoltage shutdown/undervoltage lockout
- Thermal shutdown

Description

The PWR-SMP3, intended for off-line isolated power supply applications, combines a high voltage power MOSFET switch with a switchmode power system controller in a monolithic integrated circuit. Few external components are required to implement a low cost, isolated, off-line power supply. High frequency operation reduces total power supply size.

The power MOSFET switch features include high voltage, low $R_{DS(ON)}$, low capacitance, and low gate threshold voltage. The combination of lower capacitance, and lower gate threshold voltage results in a reduction in gate drive power. Lower capacitances also facilitate higher frequency operation.

The controller section of the PWR-SMP3 contains all the blocks required to drive and control the power stage: off-line start-up pre-regulator circuit, oscillator, bandgap reference voltage, error amplifier, gate driver, undervoltage lockout, over-temperature protection, and current limiting. This voltage-mode Pulse Width Modulation control circuit is optimized for flyback topologies.

The PWR-SMP3 is available in a 16-pin plastic DIP package.

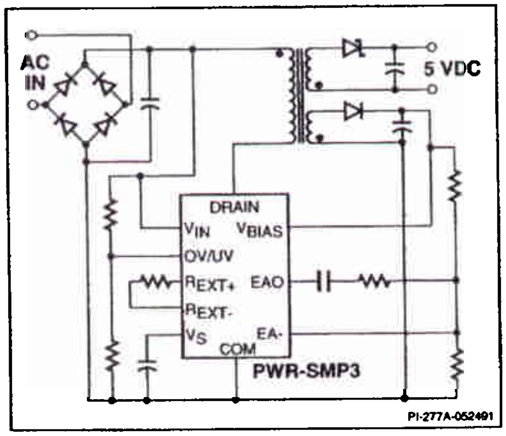

Figure 1. Typical Application

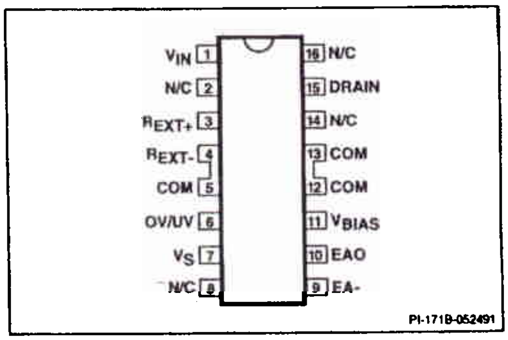

Figure 2. Pin Configuration

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ORDERING INFORMATION		
PART NUMBER	PACKAGE	TEMP RANGE
PWR-SMP3BNC	16-pin PWR PDIP	0 to 70°C

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Pin Functional Description

Pin 1:
High voltage V_{IN} for connection to the high voltage pre-regulator used to self-power the device during start-up.

Pin 2:
N/C for creepage distance.

Pin 3:
A resistor placed between R_{EXT+} and R_{EXT}- sets the internal bias currents.

Pin 4:
R_{EXT-} is the return for the reference current. Do not connect to ground plane.

Pin 5, 12, 13:
COM connections. Ground or reference point for the circuit.

Pin 6:
OV/UV is used with an external resistor divider to shut down the power supply when the input voltage is not within the desired range.

Pin 7:
Connection for a bypass capacitor for the internally generated V_S supply.

Pin 8:
N/C

Pin 9:
EA– is the error amplifier inverting input for connection to the external feedback and compensation networks.

Pin 10:
EAO is the error amplifier output for connection to the external compensation network.

Pin 11:
V_{BIAS} is the feedback voltage used to self-power the device once the supply is operating.

Pin 14:
N/C for creepage distance.

Pin 15:
Open **DRAIN** of the output MOSFET.

Pin 16:
N/C for creepage distance.

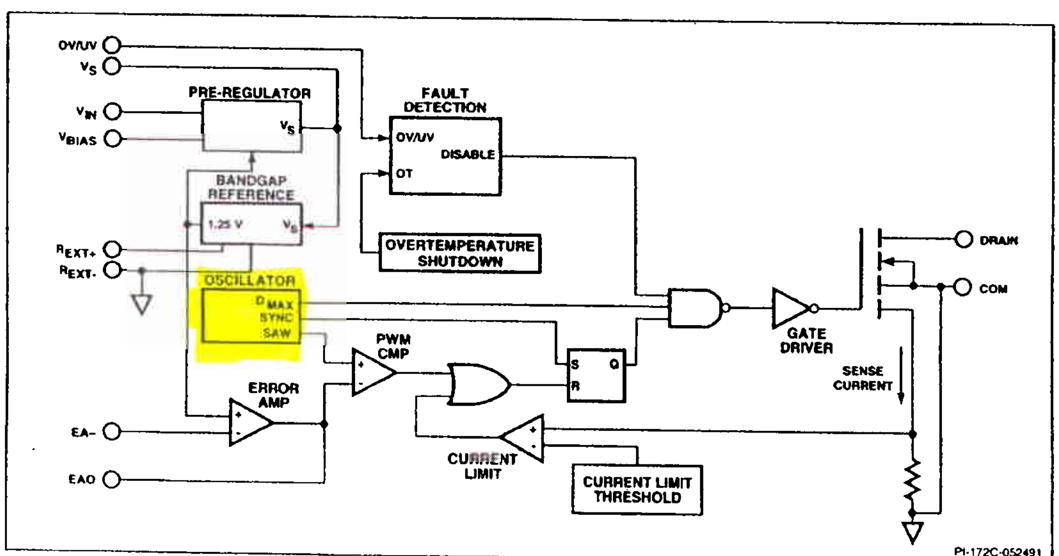

Figure 3. Functional Block Diagram of the PWR-SMP3.

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PWR-SMP3 Functional Description

Pre-regulator and On-board Voltages
The pre-regulator provides the bias current required by the controller and driver circuitry. The pre-regulator consists of a high voltage MOSFET, a gate bias current source, and an error amplifier. The error amplifier regulates V_S to approximately 5.6 volts by controlling the gate of the MOSFET.

The pre-regulator MOSFET dissipates significant amounts of power when supplying bias current. This dissipation is eliminated when the feedback winding and filter drives the V_{BIAS} pin above 8.25 volts. The pre-regulator is then cut off and internal bias current is supplied by the feedback circuit connected to V_{BIAS}.

V_S is the supply voltage for the controller and driver circuitry. An external bypass capacitor connected to V_S is required for filtering and reducing noise.

Band Gap Reference
V_{REF} is the 1.25 V reference voltage generated by the temperature-compensated bandgap reference and buffer. This voltage is used for setting thresholds for the error amplifier, over temperature circuit, and current limit circuit.

Oscillator
The oscillator is completely self-contained. An internal capacitor is alternately charged and discharged by switched constant current sources.

The voltage switch points are determined by hysteresis built into a comparator. The period of the waveform is determined by values of the current sources which set the rising and falling slopes of the sawtooth waveform. Maximum duty cycle is equal to the ratio of the charge time to the period. Clock and blanking signals are synthesized from the comparator output for use by the modulator.

Error Amplifier
The error amplifier consists of a high performance operational amplifier with the non-inverting input connected to the internal bandgap reference voltage. The output of the error amplifier directly controls the duty cycle of the power switch.

The error amplifier output pin EAO is buffered so that external loads will not affect its output. The buffer has an offset voltage of around 2 V, and an output impedance of around 1.5 kΩ.

Pulse Width Modulator
The pulse width modulator implements a voltage-mode control loop, and generates the digital driver signal which controls the power switch. The duty cycle of the driver signal will change as a function of input voltage and load. Increasing the duty cycle causes the power supply output voltage to go up. Conversely, decreasing the duty cycle causes the output voltage to go down. The pulse width modulator compares the control voltage (error amplifier output) with the sawtooth voltage generated by the oscillator to produce the required duty cycle.

OV/UV Lockout Protection
Undervoltage/Overvoltage Lockout disables the power switch when the input voltage is either too low or too high. A simple resistor divider to the UV/OV input will determine the voltage levels at which lockout occurs.

Overtemperature Protection
Temperature protection is provided by a precision analog circuit that turns the power switch off when the junction gets too hot (typically 135°C). The device will automatically reset and turn back on again when the junction has cooled past the hysteresis temperature level.

Current Limit Protection
The current limit sense consists of a current mirror on the power device and a sense resistor. The current mirror produces a current proportional to the drain current of the power switch. A sense voltage is generated by passing the mirror current through a sense resistor. This voltage is then compared to a reference voltage using an internal comparator.

3 W, 110 VAC Input Power Supply with Feedback Winding Regulation

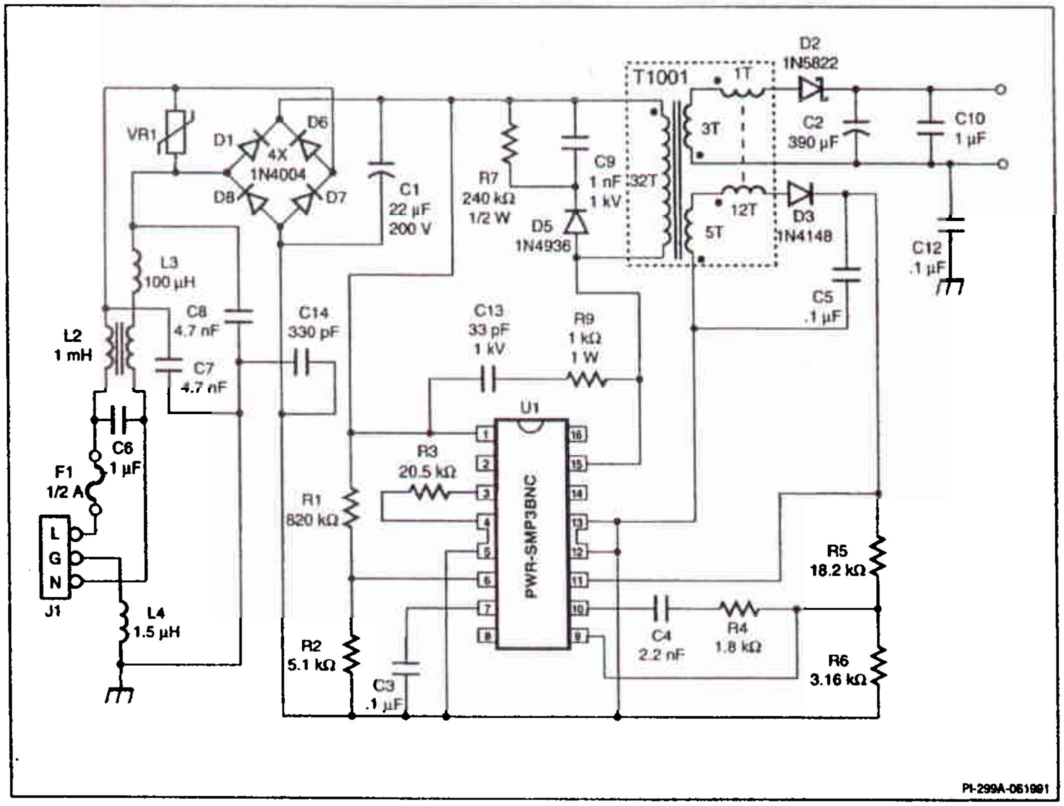


Figure 4. Schematic Diagram of a 3 W Off-line Power Supply Utilizing the PWR-SMP3. For Improved Regulation, use the Optical Feedback Circuit Shown in AN-8.

General Circuit Operation

The flyback power supply circuit shown in Figure 4, when operated with the T1001 standard transformer (see DA-3), will produce a 5 volt, 5 watt power supply that will operate from 85 to 140 V(rms) AC input voltage. The output voltage is selected by the turns ratio of the output winding to the feedback winding. The PWR-SMP3 has been designed for a feedback voltage (pin 11) of 8.5 volts. The effective turns ratio can be fine-tuned if necessary by the number of junctions in D3. Three elements affect the regulation of the output voltage; maintaining a constant feedback winding voltage, tight coupling of the power transformer, and the use of a pulse transformer to cancel the leakage inductance voltage spike.

L2, L3, L4, C6, C7, C8, C12 and C14 form an EMI filter. D1, D6, D7, D8, and C1 convert the AC input voltage to rectified DC voltage and provide the cycle-to-cycle hold-up time. D5, C9, and R7 make up a voltage clamping circuit to limit the peak voltage on the drain of the switching transistor. C13 and R9 damps the leakage inductance ringing voltage. The damping network improves the regulation of the output voltage. R5 and R6 set the feedback voltage to 8.5 volts. R4, R5, C2, C4, and T1 determine the control loop frequency response. R3 sets the current sources within the PWR-SMP3. C3 and C5 are bypass capacitors. R1 and R2 form a voltage divider network that sets the input undervoltage and overvoltage lockout trip points.

General Circuit Operation (cont.)

This circuit uses a secondary winding to monitor and regulate the output voltage. This technique can provide regulation and stability of ±5%. If tighter regulation is required for a given application, an optical feedback technique can be used. See AN-8 for further information on optical feedback.

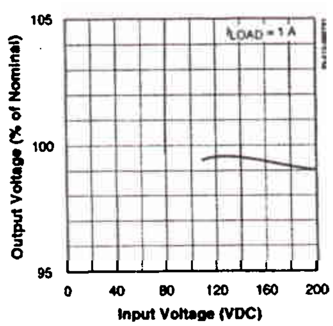
The circuit shown in Figure 4 is the schematic diagram of the PWR-EVAL1 evaluation board. This completely assembled and tested board can be ordered directly from Power Integrations, Inc. for evaluation of the PWR-SMP3. Complete supply specifications are included, as well as instructions on how to modify the board for other output voltages and oscillator frequencies.

The line and load regulation graphs shown below were measured on a PWR-EVAL1 board operated from a DC source. The switching frequency of the power supply was measured at 950 kHz.

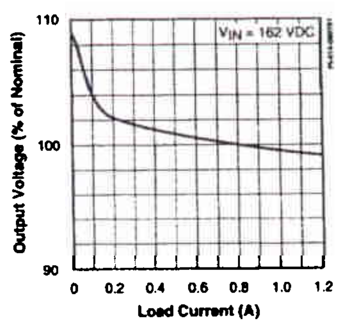
The maximum output power curve shows the power output capability for the standard transformer T1001. See DA-3 for further information on ordering transformers for use with the PWR-SMP3.

Typical Performance Characteristics (Figure 4 Power Supply)

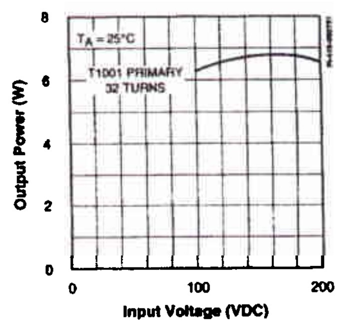
LINE REGULATION



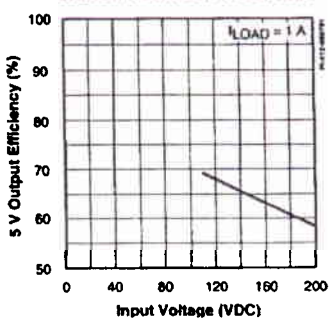
LOAD REGULATION



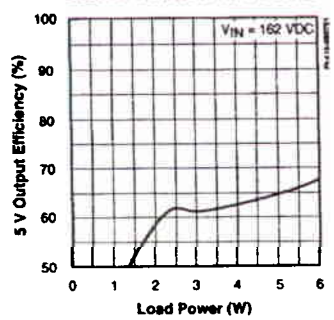
MAXIMUM OUTPUT POWER



EFFICIENCY vs. INPUT VOLTAGE



EFFICIENCY vs. OUTPUT POWER



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ABSOLUTE MAXIMUM RATINGS

Drain Voltage .... 350 V
V_{IN} Voltage .... 350 V
V_{BIAS} Voltage .... 11 V
Drain Current[2] .... 700 mA
Input Voltage[3] .... - 0.3 V to V_S + 0.3 V
Storage Temperature .... –65 to 125°C
Ambient Temperature .... 0 to 70°C
Junction Temperature[2] .... 150°C
Lead Temperature[4] .... 260°C

Power Dissipation (T_A = 25°C) .... 2.1 W
(T_A = 70°C) .... 1.05 W
Thermal Impedance (θ_{JA}) .... 43°C/W
Thermal Impedance (θ_{JC})[5] .... 6°C/W

1. Unless noted, all voltages referenced to COM.
2. Normally limited by internal circuitry.
3. Does not apply to V_{IN} or DRAIN.
4. 1/16" from case for 5 seconds.
5. Measured at pin 12/13.

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 160 V, V_{BIAS} = 8.5 V, COM = 0 V, R_{EXT} = 20.5 kΩ, T_A = 0 to 70°C	Test Limits MIN	TYP	MAX	Units
OSCILLATOR						
Output Frequency	f_{OSC}		800	950	1100	kHz
PULSE WIDTH MODULATOR						
Duty Cycle	DC		0-35	0-39		%
CIRCUIT PROTECTION						
Current Limit Threshold			350	425	500	mA
Input UV Trip-off			0.29	0.34	0.39	V
Input UV Hysteresis			35	50	70	mV
Input OV Trip-off		See Note 1	1.17	1.25	1.33	V
Input OV Hysteresis			40	60	80	mV
OV/UV Turn-off Delay Time	$t_{d(off)}$	See Figure 5		250	500	ns
Thermal Shutdown Temperature			115	135		°C
Thermal Shutdown Hysteresis				45		°C

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Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 160 V, V_{BIAS} = 8.5 V, COM = 0 V R_{EXT} = 20.5 kΩ T_A = 0 to 70°C		Test Limits MIN	TYP	MAX	Units
ERROR AMPLIFIER							
Reference Voltage	V_{REF}			1.21	1.25	1.29	V
Reference Voltage Temperature Drift	ΔV_{REF}				50		ppm/°C
Gain-Bandwidth Product				0.9	1.0		MHz
DC Gain	A_{VOL}			60	80		dB
Output Impedance	Z_{OUT}				1.5		kΩ
OUTPUT							
ON-State Resistance	$R_{DS(ON)}$	I_D = 100 mA	T_j = 25°C		14	16	Ω
			T_j = 115°C		21	25	
ON-State Current	$I_{D(ON)}$	V_{DS} = 10 V		280			mA
OFF-State Current	I_{DSS}	V_{DRAIN} = 280 V, T_A = 115°C			10	25	μA
Breakdown Voltage	BV_{DSS}	I_D = 100 μA, T_A = 25°C		350			V
Output Capacitance	C_{OSS}	V_{DRAIN} = 25 V, f = 1 MHz			22		pF
Output Stored Energy	E_{OSS}	V_{DRAIN} = 200 V			170		nJ
Rise Time	t_R	See Figure 5			33	100	ns
Fall Time	t_F	See Figure 5			8	15	ns
SUPPLY							
Pre-regulator Voltage	V_{IN}			36		350	V

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Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 160 V, V_{BIAS} = 8.5 V, COM = 0 V, R_{EXT} = 20.5 kΩ, T_A = 0 to 70°C	Test Limits MIN	TYP	MAX	Units
SUPPLY (cont.)						
Pre-regulator Cutoff Voltage	$V_{BIAS(CO)}$		6.5		8.25	V
Off-line Supply Current	I_{IN}	V_{BIAS} not connected		4	5.0	mA
		V_{BIAS} > 8.25 V			0.1	
V_{BIAS} Supply Voltage	V_{BIAS}	V_{BIAS} externally supplied via feedback	8.25		9.0	V
V_{BIAS} Supply Current	I_{BIAS}	V_{BIAS} externally supplied via feedback		4	5.0	mA
V_S Source Voltage	V_S		5.1		6.0	V
V_S Source Current	I_S				400	µA

NOTES:

1. Applying >3.5 V to the OV/UV pin activates an internal test circuit that turns on the output switch continuously. Destruction of the part can occur if the output of the PWR-SMP3 is connected to a high voltage power source when the test circuit is activated.

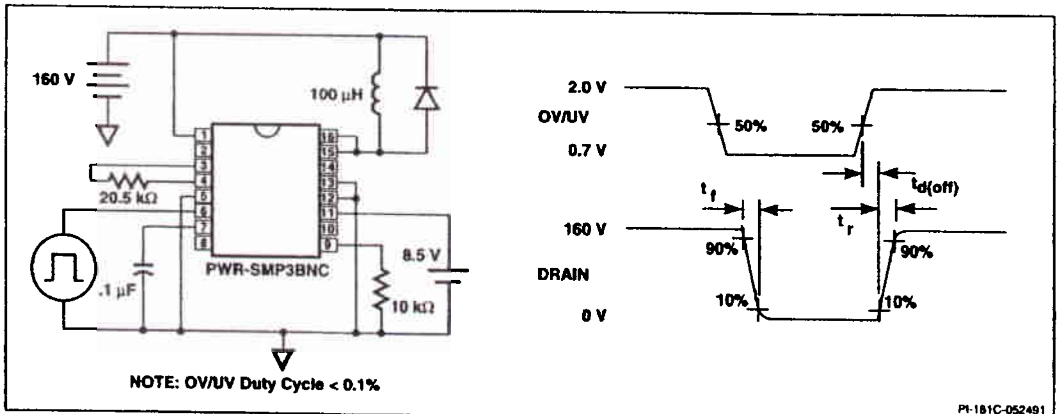

Figure 7. Switching Time Test Circuit

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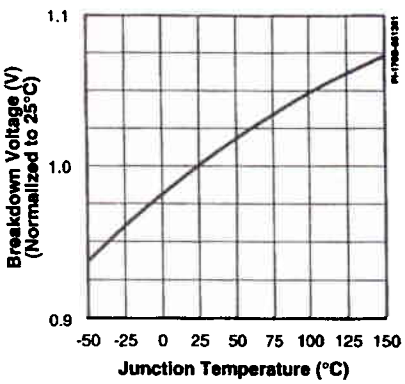
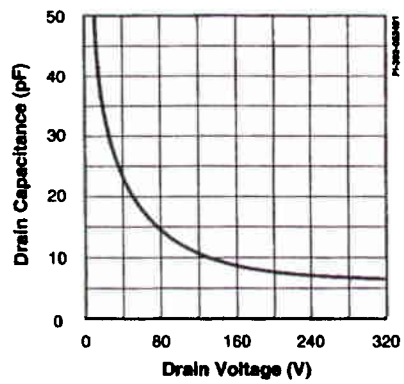
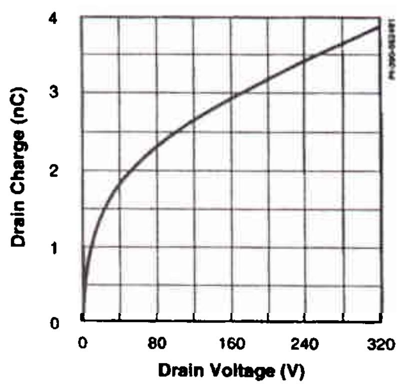
BREAKDOWN vs. TEMPERATURE



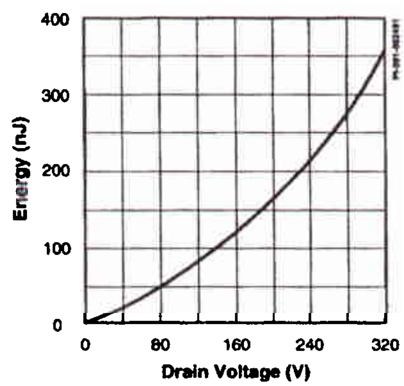
C_{OSS} vs. DRAIN VOLTAGE



DRAIN CHARGE vs. DRAIN VOLTAGE



DRAIN CAPACITANCE ENERGY



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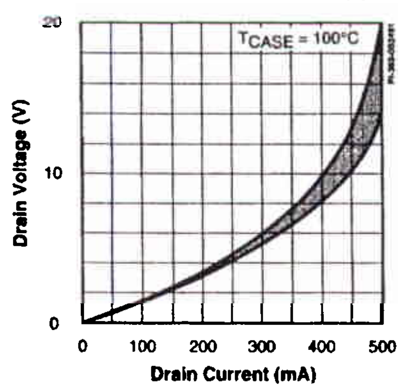
TRANSFER CHARACTERISTICS



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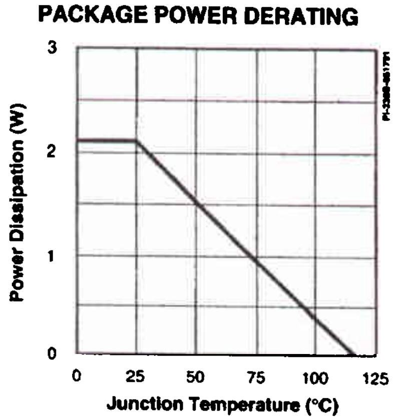
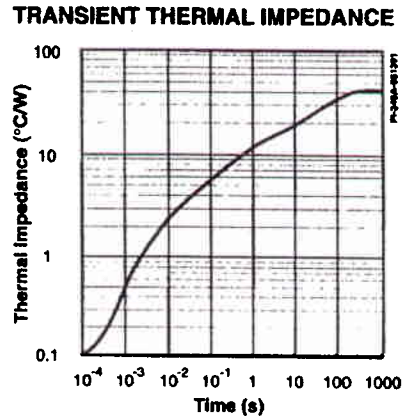

PACKAGE POWER DERATING
Power Dissipation (W)
3
2
1
0
0
25
50
75
100
125
Junction Temperature (°C)


TRANSIENT THERMAL IMPEDANCE
Thermal Impedance (°C/W)
100
10
1
0.1
10-4
10-3
10-2
10-1
1
10
100
1000
Time (s)

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